

```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 33
description:
top level BOM
-----
revision 3.740
date: 1995/05/18 19:10:16;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Release removal of the nasties
-----
revision 3.739
date: 1995/05/18 18:58:59;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Clean build, Fix to hernmasty
-----
revision 3.738
date: 1995/05/18 18:58:33;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
    Makefile.vo

This missed BOM 307 but is needed for a good top level run
-----
revision 3.737
date: 1995/05/18 18:39:28;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify
    Makefile.rules

Added default target of all for those Makefiles in stb that do not have one.
-----
revision 3.736
date: 1995/05/18 17:42:53;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/perf

Clean build
-----
revision 3.735
date: 1995/05/18 17:30:19;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hcpll

Clean build
-----
revision 3.734
date: 1995/05/18 17:23:34;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/ce

Build rom tests
-----
revision 3.733
```

date: 1995/05/18 08:04:54; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through register writes of src!=dst GGFMul to allow NB load data return preempt to satisfy dependency of only the 2nd high half of a GGFMul source register pair. Create a hole in GGFMul's repel state to do this. The april95 version of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis. Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present, eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors in the hz to cdio strNdx path; while at it making ctiod receiver of same hr too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 3.732  
date: 1995/05/18 07:20:43; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions at 900ps

---

revision 3.731  
date: 1995/05/18 07:18:51; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions at 900ps

---

revision 3.730  
date: 1995/05/18 07:16:53; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions at 900ps

---

revision 3.729  
date: 1995/05/18 07:15:04; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions at 900ps

---

revision 3.728  
date: 1995/05/17 22:27:02; author: woody; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/uu

Placement change to help top-level routing. Reduced congestion in center area around instUR/nb dependency stuff. Used up more of the empty space in the first

4 rows.

```
Atoms:           count atom  bjt  isrc  pld  clock
BJT Totals:     3834  27758 59276 45685 38424 18136

**** converged in 3 iterations ****
-----
revision 3.727
date: 1995/05/17 20:52:52; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/doc/debug
    Simulator_configuration.mif

Added Title
-----
revision 3.726
date: 1995/05/17 20:29:01; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/doc/debug

How to do debug in the gate level simulator environment. Basic
course.
-----
revision 3.725
date: 1995/05/17 00:53:34; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctioi

ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
    Power up RAM read index from f4s to f24s per recent analysis.
-----
revision 3.724
date: 1995/05/16 22:43:34; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cj

Last release was supposed to be dot-zero.
-----
revision 3.723
date: 1995/05/16 22:40:30; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
    cust_intf.wkz

cj/cj.pim cj/genptab.pl cust_intf.wkz
-----
revision 3.722
date: 1995/05/16 22:39:30; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cj
    cj.pim
    genptab.pl

cj/cj.pim cj/genptab.pl cust_intf.wkz:
    Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
-----
revision 3.721
date: 1995/05/16 18:20:36; author: bobm; state: Exp; lines: +2 -2
Release Target: euterpe/doc
    pipeline.mif
```

WAIT WAIT...There's one more little half-sentence change. We can't

have a release without one more last second change. Blame this  
one on billz. :-)

---

revision 3.720  
date: 1995/05/16 17:58:01; author: bobm; state: Exp; lines: +2 -2  
Release Target: euterpe/doc  
    Makefile  
    euterpe-microarch.book  
    front.mif  
    euterpe-microarchTOC.mif  
    intro.mif  
    opcodes.mif  
    pipeline.mif  
    memory.mif  
    events.mif  
    reset.mif  
    clock.mif  
    cerberus.mif  
     endian.mif  
    newchanges.mif

Version 1.9 of Euterpe MicroArchitecture.

---

revision 3.719  
date: 1995/05/16 08:03:06; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/ctiod

Part of cdio/ctiod/euterpe.V checkin.

~

---

revision 3.718  
date: 1995/05/16 07:58:49; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cdio

Part of cdio/ctiod/euterpe.V checkin.

~

---

revision 3.717  
date: 1995/05/16 05:01:41; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc  
    Makefile.vo

deleted obsolete .hwc rule. remove rsh from all gards jobs

---

revision 3.716  
date: 1995/05/16 01:55:40; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/uu  
    uu\_control.pim

uu/uu\_control.pim: Placement for recent uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn.

---

revision 3.715  
date: 1995/05/16 01:07:43; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/uu  
    uu.V  
    uuprblmr13.Veqn

uuprblmwm.Veqn

uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:  
Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode  
was forgotten, allowing the PC to increment before being saved by event entry.  
Test cachenasty5\_0 noticed with a D cache miss hiccup. Placement later.

-----

revision 3.714  
date: 1995/05/15 22:19:00; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/ld

Cosmetic changes to Makefile

-----

revision 3.713  
date: 1995/05/15 20:55:24; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/include

end.S now needs cerberus.h  
Uses new positions of end, status, and print octlets for \_2 tests.

-----

revision 3.712  
date: 1995/05/15 20:43:57; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel

Fixed cerberus gtlb entry for work for \_2 versions of memory management tests.  
Added cachenasty5 and hermnasty.  
Fixed Makefile for config1 rules.

-----

revision 3.711  
date: 1995/05/15 20:13:22; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify  
    Makefile.defs  
    Makefile.rules

Added hconfig rules, moved defs from toplevel

-----

revision 3.710  
date: 1995/05/13 17:58:57; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

Consolidate to .0 BOM for next major snapshot update.

Several small placement tweaks (this version might make it through  
second iteration placement . . .).

Tau phase bug fix in uu - this is a logic change.

-----

revision 3.709  
date: 1995/05/13 17:40:40; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/gf

shift left 18 atoms to prevent clash with cr

-----

revision 3.708  
date: 1995/05/13 12:33:31; author: tbr; state: Exp; lines: +2 -2

```
Release Target: euterpe/verilog/bsrc
    Makefile.tst

correct syntax error in last change
=====

RCS file: /s6/cvsroot/euterpe/doc/BOM,v
Working file: doc/BOM
head: 22.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;      selected revisions: 4
description:
BOM for doc
-----
revision 19.7
date: 1995/05/17 20:52:37;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc/debug
    Simulator_configuration.mif

Added Title
-----
revision 19.6
date: 1995/05/17 20:28:41;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/doc/debug

How to do debug in the gate level simulator environment. Basic
course.
-----
revision 19.5
date: 1995/05/16 18:20:08;  author: bobm;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
    pipeline.mif

WAIT WAIT...There's one more little half-sentence change.  We can't
have a release without one more last second change.  Blame this
one on billz. :-(

-----
revision 19.4
date: 1995/05/16 17:57:36;  author: bobm;  state: Exp;  lines: +21 -13
Release Target: euterpe/doc
    Makefile
    euterpe-microarch.book
    front.mif
    euterpe-microarchTOC.mif
    intro.mif
    opcodes.mif
    pipeline.mif
    memory.mif
    events.mif
    reset.mif
    clock.mif
    cerberus.mif
    endian.mif
```

newchanges.mif

Version 1.9 of Euterpe MicroArchitecture.

---

RCS file: /s6/cvsroot/euterpe/doc/Attic/EuterpeDebug.html,v  
Working file: doc/EuterpeDebug.html  
head: 19.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1; selected revisions: 1  
description:  
-----  
revision 19.1  
date: 1995/05/16 00:43:52; author: jeffm; state: Exp;  
Instructions on using a likedriverlog, and supporting logfiles, to  
debug problems during Euterpe simulation.

---

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v  
Working file: doc/cerberus.mif  
head: 4.39  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 53; selected revisions: 1  
description:  
-----  
revision 4.35  
date: 1995/05/16 17:46:08; author: bobm; state: Exp; lines: +357 -314  
Version 1.9 of the Euterpe MicroArchitecture book.  
Post-review version.

---

RCS file: /s6/cvsroot/euterpe/doc/Attic/clock.mif,v  
Working file: doc/clock.mif  
head: 19.6  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 6; selected revisions: 1  
description:  
-----  
revision 19.5  
date: 1995/05/16 17:45:50; author: bobm; state: Exp; lines: +62 -86  
Version 1.9 of the Euterpe MicroArchitecture book.  
Post-review version.

---

RCS file: /s6/cvsroot/euterpe/doc/Attic/endian.mif,v  
Working file: doc/endian.mif  
head: 19.6

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 19.5
date: 1995/05/16 17:46:29;  author: bobm;  state: Exp;  lines: +103 -124
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====
RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarch.book,v
Working file: doc/euterpe-microarch.book
head: 4.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;      selected revisions: 1
description:
-----
revision 4.13
date: 1995/05/16 17:40:18;  author: bobm;  state: Exp;  lines: +6 -7
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====
RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarchTOC.mif,v
Working file: doc/euterpe-microarchTOC.mif
head: 4.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;      selected revisions: 1
description:
-----
revision 4.14
date: 1995/05/16 17:40:27;  author: bobm;  state: Exp;  lines: +412 -411
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====
RCS file: /s6/cvsroot/euterpe/doc/Attic/events.mif,v
Working file: doc/events.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;      selected revisions: 1
description:
-----
revision 4.23
date: 1995/05/16 17:45:34;  author: bobm;  state: Exp;  lines: +350 -116
....
```

Version 1.9 of the Euterpe MicroArchitecture book.  
Post-review version.

```
=====
```

RCS file: /s6/cvsroot/euterpe/doc/Attic/front.mif,v  
Working file: doc/front.mif  
head: 16.8  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 8; selected revisions: 1  
description:  
-----  
revision 16.8  
date: 1995/05/16 17:40:21; author: bobm; state: Exp; lines: +27 -27  
Version 1.9 of the Euterpe MicroArchitecture book.  
Post-review version.

```
=====
```

RCS file: /s6/cvsroot/euterpe/doc/Attic/intro.mif,v  
Working file: doc/intro.mif  
head: 4.22  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 26; selected revisions: 1  
description:  
-----  
revision 4.21  
date: 1995/05/16 17:40:37; author: bobm; state: Exp; lines: +728 -690  
Version 1.9 of the Euterpe MicroArchitecture book.  
Post-review version.

```
=====
```

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v  
Working file: doc/memory.mif  
head: 4.36  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 46; selected revisions: 1  
description:  
-----  
revision 4.33  
date: 1995/05/16 17:45:12; author: bobm; state: Exp; lines: +1579 -804  
Version 1.9 of the Euterpe MicroArchitecture book.  
Post-review version.

```
=====
```

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v  
Working file: doc/newchanges.mif  
head: 16.13  
branch:  
locks: strict

```
access list:
keyword substitution: kv
total revisions: 13;      selected revisions: 1
description:
-----
revision 16.11
date: 1995/05/16 17:46:33;  author: bobm;  state: Exp;  lines: +69 -28
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/opcodes.mif,v
Working file: doc/opcodes.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;      selected revisions: 1
description:
-----
revision 4.23
date: 1995/05/16 17:44:04;  author: bobm;  state: Exp;  lines: +19 -19
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/pipeline.mif,v
Working file: doc/pipeline.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;      selected revisions: 2
description:
-----
revision 4.23
date: 1995/05/16 18:18:47;  author: bobm;  state: Exp;  lines: +152 -152
small consistency change for late dirty cache misses
-----
revision 4.22
date: 1995/05/16 17:44:49;  author: bobm;  state: Exp;  lines: +1266 -903
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/reset.mif,v
Working file: doc/reset.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;      selected revisions: 1
description:
-----
```

```
revision 4.21
date: 1995/05/16 17:45:43; author: bobm; state: Exp; lines: +66 -39
Version 1.9 of the Euterpe MicroArchitecture book.
Post-review version.
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/BOM,v
Working file: doc/debug/BOM
head: 3.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4; selected revisions: 3
description:
releasebom adding BOM
-----
revision 2.1
date: 1995/05/17 20:52:28; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/doc/debug
    Simulator_configuration.mif

Added Title
-----
revision 2.0
date: 1995/05/17 20:28:28; author: jeffm; state: Exp; lines: +1 -1
Release Target: euterpe/doc/debug

How to do debug in the gate level simulator environment. Basic
course.
-----
revision 1.1
date: 1995/05/17 20:28:21; author: jeffm; state: Exp;
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/DebugExample_bad.html,v
Working file: doc/debug/DebugExample_bad.html
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1; selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:25:43; author: jeffm; state: Exp;
Rev 0 checking of the complete package.
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/DebugExample_head.html,v
Working file: doc/debug/DebugExample_head.html
head: 1.1
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:25:45;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====

RCS file: /s6/cvsroot/euterpe/doc/debug/DebugExample_llev.html,v
Working file: doc/debug/DebugExample_llev.html
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:25:46;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====

RCS file: /s6/cvsroot/euterpe/doc/debug/DebugExample_llnav.html,v
Working file: doc/debug/DebugExample_llnav.html
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:25:48;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====

RCS file: /s6/cvsroot/euterpe/doc/debug/DebugExample_nav.html,v
Working file: doc/debug/DebugExample_nav.html
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:25:51;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====

RCS file: /s6/cvsroot/euterpe/doc/debug/DebugExample_xcor.html,v
Working file: doc/debug/DebugExample_xcor.html
head: 1.1
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:25:52;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/EuterpeDebug.html,v
Working file: doc/debug/EuterpeDebug.html
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 4
description:
-----
revision 1.4
date: 1995/05/17 20:25:54;  author: jeffm;  state: Exp;  lines: +48 -41
Rev 0 checking of the complete package.
-----
revision 1.3
date: 1995/05/16 23:01:40;  author: lisar;  state: Exp;  lines: +15 -11
Added confidential header, and simtick info.
-----
revision 1.2
date: 1995/05/16 22:24:11;  author: jeffm;  state: Exp;  lines: +30 -12
Added lots of stuff.
-----
revision 1.1
date: 1995/05/16 19:17:37;  author: jeffm;  state: Exp;
Initial Checking in debug directory.
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/EuterpeDebug_not_obv.html,v
Working file: doc/debug/EuterpeDebug_not_obv.html
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 1.2
date: 1995/05/17 20:25:56;  author: jeffm;  state: Exp;  lines: +136 -28
Rev 0 checking of the complete package.
-----
revision 1.1
date: 1995/05/16 19:17:38;  author: jeffm;  state: Exp;
Initial Checking in debug directory.
=====
```

```
RCS file: /s6/cvsroot/euterpe/doc/debug/EuterpeDebug_obv.html,v
Working file: doc/debug/EuterpeDebug_obv.html
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 1.2
date: 1995/05/17 20:25:58;  author: jeffm;  state: Exp;  lines: +18 -3
Rev 0 checking of the complete package.
-----
revision 1.1
date: 1995/05/16 19:17:40;  author: jeffm;  state: Exp;
Initial Checking in debug directory.
=====

RCS file: /s6/cvsroot/euterpe/doc/debug/EuterpeDebug_pipe.html,v
Working file: doc/debug/EuterpeDebug_pipe.html
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:26:00;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====

RCS file: /s6/cvsroot/euterpe/doc/debug/Logfiles.html,v
Working file: doc/debug/Logfiles.html
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 4
description:
-----
revision 1.4
date: 1995/05/17 20:26:01;  author: jeffm;  state: Exp;  lines: +28 -9
Rev 0 checking of the complete package.
-----
revision 1.3
date: 1995/05/16 23:01:41;  author: lisar;  state: Exp;  lines: +16 -4
Added confidential header, and simtick info.
-----
revision 1.2
date: 1995/05/16 21:26:52;  author: lisar;  state: Exp;  lines: +17 -4
Just more formatting.
=====
```

```
revision 1.1
date: 1995/05/16 19:12:26;  author: lisar;  state: Exp;
Initial revision
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/Simulator_configuration.mif,v
Working file: doc/debug/Simulator_configuration.mif
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 5
description:
-----
revision 1.5
date: 1995/05/17 20:52:13;  author: lisar;  state: Exp;  lines: +351 -274
Added Title
-----
revision 1.4
date: 1995/05/17 19:15:29;  author: lisar;  state: Exp;  lines: +36 -6
Correct spelling
-----
revision 1.3
date: 1995/05/17 19:13:01;  author: lisar;  state: Exp;  lines: +2301 -121
Added runtimes and results
-----
revision 1.2
date: 1995/05/16 23:01:43;  author: lisar;  state: Exp;  lines: +144 -11
Added confidential header, and simtick info.
-----
revision 1.1
date: 1995/05/16 22:20:51;  author: lisar;  state: Exp;
Euterpe simulation
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/likedriverlog_flds.html,v
Working file: doc/debug/likedriverlog_flds.html
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 1.2
date: 1995/05/17 20:26:03;  author: jeffm;  state: Exp;  lines: +36 -11
Rev 0 checking of the complete package.
-----
revision 1.1
date: 1995/05/16 19:17:41;  author: jeffm;  state: Exp;
Initial Checking in debug directory.
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/likedriverlog_nav.html,v
Working file: doc/debug/likedriverlog_nav.html
```

```
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 1.2
date: 1995/05/17 20:26:05;  author: jeffm;  state: Exp;  lines: +113 -0
Rev 0 checking of the complete package.
-----
revision 1.1
date: 1995/05/16 19:17:43;  author: jeffm;  state: Exp;
Initial Checking in debug directory.
=====
RCS file: /s6/cvsroot/euterpe/doc/debug/likedriverlog_x.html,v
Working file: doc/debug/likedriverlog_x.html
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/17 20:26:07;  author: jeffm;  state: Exp;
Rev 0 checking of the complete package.
=====
RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;      selected revisions: 10
description:
-----
revision 4.118
date: 1995/05/18 19:09:57;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Release removal of the nasties
-----
revision 4.117
date: 1995/05/18 18:58:43;  author: lisar;  state: Exp;  lines: +5 -1
Release Target: euterpe/verify/nasty

Clean build, Fix to hernmasty
-----
revision 4.116
date: 1995/05/18 18:39:12;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify
```

Makefile.rules

Added default target of all for those Makefiles in stb that do not have one.  
-----

revision 4.115  
date: 1995/05/18 17:42:39; author: lisar; state: Exp; lines: +5 -1  
Release Target: euterpe/verify/perf

Clean build

-----

revision 4.114  
date: 1995/05/18 17:30:05; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/hcp11

Clean build

-----

revision 4.113  
date: 1995/05/18 17:23:20; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/ce

Build rom tests

-----

revision 4.112  
date: 1995/05/15 22:18:45; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/standalone/ld

Cosmetic changes to Makefile

-----

revision 4.111  
date: 1995/05/15 20:55:00; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/include

end.S now needs cerberus.h  
Uses new positions of end, status, and print octlets for \_2 tests.

-----

revision 4.110  
date: 1995/05/15 20:43:41; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel

Fixed cerberus gtlb entry for work for \_2 versions of memory management tests.  
Added cachenasty5 and hermnasty.  
Fixed Makefile for config1 rules.

-----

revision 4.109  
date: 1995/05/15 20:13:05; author: lisar; state: Exp; lines: +3 -3  
Release Target: euterpe/verify  
    Makefile.defs  
    Makefile.rules

Added hconfig rules, moved defs from toplevel

=====

RCS file: /s6/cvsroot/euterpe/verify/Makefile,v  
Working file: verify/Makefile  
head: 3.25  
branch:

```
locks: strict
access list:
keyword substitution: kv
total revisions: 25;      selected revisions: 3
description:
-----
revision 3.15
date: 1995/05/18 22:39:34;  author: dit00;  state: Exp;  lines: +5 -5
Moved stb dependancy to where its actually needed
-----
revision 3.14
date: 1995/05/18 18:54:52;  author: lisar;  state: Exp;  lines: +10 -2
Added hcpl1 and perf
-----
revision 3.13
date: 1995/05/16 00:13:22;  author: jeffm;  state: Exp;  lines: +6 -1
Add nasty test directory to build.
=====
RCS file: /s6/cvsroot/euterpe/verify/Makefile.defs,v
Working file: verify/Makefile.defs
head: 1.43
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 43;      selected revisions: 1
description:
-----
revision 1.38
date: 1995/05/15 20:12:27;  author: lisar;  state: Exp;  lines: +16 -3
rules:
    Added hconfig

defs:
    Moved defs from toplevel
=====
RCS file: /s6/cvsroot/euterpe/verify/Makefile.rules,v
Working file: verify/Makefile.rules
head: 1.72
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;      selected revisions: 2
description:
-----
revision 1.66
date: 1995/05/18 18:38:56;  author: lisar;  state: Exp;  lines: +4 -1
Added default target of all for those Makefiles in stb that do not have one.
-----
revision 1.65
date: 1995/05/15 20:12:29;  author: lisar;  state: Exp;  lines: +8 -1
rules:
    Added hconfig
```

```
defs:
    Moved defs from toplevel
=====
RCS file: /s6/cvsroot/euterpe/verify/status,v
Working file: verify/status
head: 3.64
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 64;    selected revisions: 1
description:
-----
revision 3.24
date: 1995/05/15 12:08:02;  author: lisar;  state: Exp;  lines: +2792 -0
Periodic checkin
=====
RCS file: /s6/cvsroot/euterpe/verify/include/BOM,v
Working file: verify/include/BOM
head: 36.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 29.0
date: 1995/05/15 20:54:42;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/include

end.S now needs cerberus.h
Uses new positions of end, status, and print octlets for _2 tests.
-----
revision 28.1
date: 1995/05/15 20:54:32;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/verify/include/Makefile,v
Working file: verify/include/Makefile
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
-----
revision 1.15
date: 1995/05/18 23:41:21;  author: jeffm;  state: Exp;  lines: +6 -4
Cleaned up some magic number usage.
Added macros for getting base addresses for any cerberus net and node.
Added macro to get the cerberus space address, independent of what
```

euterpe's base is.  
Added macro to get the address of the parity error forcing octlet in snoopy.

---

RCS file: /s6/cvsroot/euterpe/verify/include/end.S,v  
Working file: verify/include/end.S  
head: 1.38  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 38; selected revisions: 1  
description:  
-----  
revision 1.33  
date: 1995/05/18 23:41:23; author: jeffm; state: Exp; lines: +31 -84  
Cleaned up some magic number usage.  
Added macros for getting base addresses for any cerberus net and node.  
Added macro to get the cerberus space address, independent of what  
euterpe's base is.  
Added macro to get the address of the parity error forcing octlet in snoopy.

---

RCS file: /s6/cvsroot/euterpe/verify/include/physaddr.h,v  
Working file: verify/include/physaddr.h  
head: 4.24  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 24; selected revisions: 1  
description:  
-----  
revision 4.23  
date: 1995/05/18 23:41:26; author: jeffm; state: Exp; lines: +50 -8  
Cleaned up some magic number usage.  
Added macros for getting base addresses for any cerberus net and node.  
Added macro to get the cerberus space address, independent of what  
euterpe's base is.  
Added macro to get the address of the parity error forcing octlet in snoopy.

---

RCS file: /s6/cvsroot/euterpe/verify/lib/Makefile,v  
Working file: verify/lib/Makefile  
head: 1.16  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 16; selected revisions: 1  
description:  
-----  
revision 1.15  
date: 1995/05/18 23:41:21; author: jeffm; state: Exp; lines: +6 -4  
Cleaned up some magic number usage.  
Added macros for getting base addresses for any cerberus net and node.  
Added macro to get the cerberus space address, independent of what

euterpe's base is.  
Added macro to get the address of the parity error forcing octlet in snoopy.

```
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/.checkoutrc,v
Working file: verify/nasty/.checkoutrc
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 18:57:55;  author: lisar;  state: Exp;
Clean build
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/BOM,v
Working file: verify/nasty/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 36;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 2.0
date: 1995/05/18 18:58:32;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty
=====
```

Clean build, Fix to hernmasty

```
-----
```

```
revision 1.1
date: 1995/05/18 18:58:25;  author: lisar;  state: Exp;
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/Makefile,v
Working file: verify/nasty/Makefile
head: 1.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;      selected revisions: 3
description:
-----
revision 1.3
date: 1995/05/18 18:57:57;  author: lisar;  state: Exp;  lines: +2 -4
Clean build
-----
revision 1.2
date: 1995/05/16 00:08:28;  author: jeffm;  state: Exp;  lines: +39 -16
=====
```

Fixed possible race condition in the event handler.

```
-----
```

```
revision 1.1
date: 1995/05/15 20:31:40; author: jeffm; state: Exp;
Moving these from toplevel.
```

```
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty.S,v
Working file: verify/nasty/cachenasty.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:
```

```
-----
```

```
revision 1.1
date: 1995/05/15 20:31:43; author: jeffm; state: Exp;
Moving these from toplevel.
```

```
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty2.S,v
Working file: verify/nasty/cachenasty2.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:
```

```
-----
```

```
revision 1.1
date: 1995/05/15 20:31:46; author: jeffm; state: Exp;
Moving these from toplevel.
```

```
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty3.S,v
Working file: verify/nasty/cachenasty3.S
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4; selected revisions: 1
description:
```

```
-----
```

```
revision 1.1
date: 1995/05/15 20:31:49; author: jeffm; state: Exp;
Moving these from toplevel.
```

```
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty4.S,v
Working file: verify/nasty/cachenasty4.S
head: 1.4
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/15 20:31:51;  author: jeffm;  state: Exp;
Moving these from toplevel.
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5.S,v
Working file: verify/nasty/cachenasty5.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 2
description:
-----
revision 1.2
date: 1995/05/16 00:08:31;  author: jeffm;  state: Exp;  lines: +62 -5
Fixed possible race condition in the event handler.
-----
revision 1.1
date: 1995/05/15 20:31:54;  author: jeffm;  state: Exp;
Moving these from toplevel.
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty.S,v
Working file: verify/nasty/cachesynchnasty.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/15 20:31:57;  author: jeffm;  state: Exp;
Moving these from toplevel.
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2.S,v
Working file: verify/nasty/cachesynchnasty2.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/15 20:32:00;  author: jeffm;  state: Exp;
Moving these from toplevel.
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/clean-request,v
Working file: verify/nasty/clean-request
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 1.2
date: 1995/05/18 18:57:59;  author: lisar;  state: Exp;  lines: +1 -0
Clean build
-----
revision 1.1
date: 1995/05/15 20:34:38;  author: jeffm;  state: Exp;
Oops.
=====
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/hermnasty.S,v
Working file: verify/nasty/hermnasty.S
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;      selected revisions: 4
description:
-----
revision 1.4
date: 1995/05/18 18:30:24;  author: jeffm;  state: Exp;  lines: +6 -17
Fixed so that:
```

- 1) Cyl 0 can always get to the uncached hermes space 0 - so it can reset the hermes model's event registers.
- 2) Fixed cylinder 4's hermes space 0x16 gtlb entry.
- 3) Made sure that the entire line containing the event register is not touched by a cached access. Was doing a cache fill that had one blocking read.

```
-----
revision 1.3
date: 1995/05/16 00:08:33;  author: jeffm;  state: Exp;  lines: +2 -2
Fixed possible race condition in the event handler.
-----
```

```
revision 1.2
date: 1995/05/15 23:27:17;  author: jeffm;  state: Exp;  lines: +13 -3
Fixed check for rupt vs. exception to include the cylinder number.
-----
```

```
revision 1.1
date: 1995/05/15 20:32:03;  author: jeffm;  state: Exp;
Moving these from toplevel.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;  selected revisions: 2
description:
-----
revision 1.160
date: 1995/05/19 00:34:16;  author: jeffm;  state: Exp;  lines: +4 -4
Added all them aweful .hermes* files to the .cvsignore.
Removed the nasty tests from the Makefile.
Checked in the smaller prblm_debug.sig.
Fixed several tests.
-----
revision 1.159
date: 1995/05/15 20:35:57;  author: lisar;  state: Exp;  lines: +77 -81
Tidied up Makefile. Fixed config1 rules.
Bug fix in hermes_Ibash.S - still broken though.
Accessing event register when shouldn't be?
-----
RCS file: /s6/cvsroot/euterpe/verify/obj/system/nasty/Makefile,v
Working file: verify/obj/system/nasty/Makefile
head: 1.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;  selected revisions: 3
description:
-----
revision 1.3
date: 1995/05/18 18:57:57;  author: lisar;  state: Exp;  lines: +2 -4
Clean build
-----
revision 1.2
date: 1995/05/16 00:08:28;  author: jeffm;  state: Exp;  lines: +39 -16
Fixed possible race condition in the event handler.
-----
revision 1.1
date: 1995/05/15 20:31:40;  author: jeffm;  state: Exp;
Moving these from toplevel.
-----
RCS file: /s6/cvsroot/euterpe/verify/perf/.checkoutrc,v
Working file: verify/perf/.checkoutrc
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;  selected revisions: 1
description:
-----
```

```
revision 1.1
date: 1995/05/18 17:41:55; author: lisar; state: Exp;
Don't need ifdef terp
=====
RCS file: /s6/cvsroot/euterpe/verify/perf/BOM,v
Working file: verify/perf/BOM
head: 7.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13; selected revisions: 2
description:
releasebom adding BOM
-----
revision 2.0
date: 1995/05/18 17:42:30; author: lisar; state: Exp; lines: +1 -1
Release Target: euterpe/verify/perf

Clean build
-----
revision 1.1
date: 1995/05/18 17:42:25; author: lisar; state: Exp;
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/verify/perf/Makefile,v
Working file: verify/perf/Makefile
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10; selected revisions: 1
description:
-----
revision 1.2
date: 1995/05/18 17:41:57; author: lisar; state: Exp; lines: +2 -2
Don't need ifdef terp
=====
RCS file: /s6/cvsroot/euterpe/verify/perf/clean-request,v
Working file: verify/perf/clean-request
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1; selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 17:41:58; author: lisar; state: Exp;
Don't need ifdef terp
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/dcache_perf.S,v
Working file: verify/perf/dcache_perf.S
head: 1.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/05/15 18:50:02;  author: claseman;  state: Exp;  lines: +7 -16
initialize cycle count
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/dram_perf.S,v
Working file: verify/perf/dram_perf.S
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/05/18 17:41:59;  author: lisar;  state: Exp;  lines: +2 -4
Don't need ifdef terp
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/rom_perf.S,v
Working file: verify/perf/rom_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/05/18 17:42:00;  author: lisar;  state: Exp;  lines: +2 -4
Don't need ifdef terp
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/BOM,v
Working file: verify/standalone/BOM
head: 6.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;      selected revisions: 3
description:
-----
revision 4.33
date: 1995/05/18 17:29:57;  author: lisar;  state: Exp;  lines: +2 -2
```

Release Target: euterpe/verify/standalone/hcp11

Clean build

-----

revision 4.32  
date: 1995/05/18 17:23:11; author: lisar; state: Exp; lines: +5 -1

Release Target: euterpe/verify/standalone/ce

Build rom tests

-----

revision 4.31  
date: 1995/05/15 22:18:37; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/standalone/ld

Cosmetic changes to Makefile

=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/.checkoutrc,v  
Working file: verify/standalone/ce/.checkoutrc  
head: 1.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1; selected revisions: 1  
description:

-----

revision 1.1  
date: 1995/05/18 17:21:02; author: lisar; state: Exp;  
gmake

=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/BOM,v  
Working file: verify/standalone/ce/BOM  
head: 2.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 2; selected revisions: 2  
description:  
releasebom adding BOM

-----

revision 2.0  
date: 1995/05/18 17:23:00; author: lisar; state: Exp; lines: +1 -1

Release Target: euterpe/verify/standalone/ce

Build rom tests

-----

revision 1.1  
date: 1995/05/18 17:22:53; author: lisar; state: Exp;  
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/Makefile,v  
Working file: verify/standalone/ce/Makefile  
head: 1.3

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/05/18 17:15:45;  author: lisar;  state: Exp;  lines: +38 -13
Added _rom tests
=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/ce_defaults.pl,v
Working file: verify/standalone/ce/ce_defaults.pl
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/05/18 17:15:46;  author: lisar;  state: Exp;  lines: +4 -4
Added _rom tests
=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/ce_norom.S,v
Working file: verify/standalone/ce/ce_norom.S
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 17:15:47;  author: lisar;  state: Exp;
Added _rom tests
=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/ce_norom.pl,v
Working file: verify/standalone/ce/ce_norom.pl
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 17:15:49;  author: lisar;  state: Exp;
Added _rom tests
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/ce_rom.S,v
Working file: verify/standalone/ce/ce_rom.S
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 17:15:50;  author: lisar;  state: Exp;
Added _rom tests
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/ce_rom.pl,v
Working file: verify/standalone/ce/ce_rom.pl
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 17:15:51;  author: lisar;  state: Exp;
Added _rom tests
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/ce/clean-request,v
Working file: verify/standalone/ce/clean-request
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/18 17:22:18;  author: lisar;  state: Exp;
clean up
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshftshort.test,v
Working file: verify/standalone/dp/dpgshftshort.test
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 2.3
date: 1995/05/15 18:00:07;  author: veena;  state: Exp;  lines: +2 -2
```

changed bias value, so that test will not generate illegal immediate value.  
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/BOM,v  
Working file: verify/standalone/hcpll/BOM  
head: 5.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 8; selected revisions: 2  
description:  
releasebom adding BOM  
-----  
revision 4.0  
date: 1995/05/18 17:29:47; author: lisar; state: Exp; lines: +1 -1  
Release Target: euterpe/verify/standalone/hcpll

Clean build  
-----  
revision 3.1  
date: 1995/05/18 17:29:39; author: lisar; state: Exp; lines: +4 -3  
releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/Makefile,v  
Working file: verify/standalone/hcpll/Makefile  
head: 1.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 2  
description:  
-----  
revision 1.3  
date: 1995/05/18 17:29:21; author: lisar; state: Exp; lines: +5 -2  
Clean build  
-----  
revision 1.2  
date: 1995/05/18 17:26:54; author: lisar; state: Exp; lines: +24 -39  
Better rules for maing tests, cut down cases  
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/clean-request,v  
Working file: verify/standalone/hcpll/clean-request  
head: 3.2  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 2; selected revisions: 1  
description:  
-----  
revision 3.1  
date: 1995/05/18 17:29:22; author: lisar; state: Exp;  
Clean build

```
=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/hcpll.pl,v
Working file: verify/standalone/hcpll/hcpll.pl
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.2
date: 1995/05/18 17:26:56;  author: lisar;  state: Exp;  lines: +36 -66
Better rules for maing tests, cut down cases
=====
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/ife/Makefile,v
Working file: verify/standalone/ife/Makefile
head: 1.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;      selected revisions: 2
description:
-----
revision 1.19
date: 1995/05/14 00:24:14;  author: lisar;  state: Exp;  lines: +6 -4
Add ctd and cti to the all list
-----
revision 1.18
date: 1995/05/13 23:28:00;  author: lisar;  state: Exp;  lines: +7 -1
Make the cti and ctd files too
=====
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/standalone/ld/BOM,v
Working file: verify/standalone/ld/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 38;      selected revisions: 2
description:
-----
revision 18.0
date: 1995/05/15 22:18:27;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/standalone/ld
=====
```

Cosmetic changes to Makefile

```
=====
revision 17.1
date: 1995/05/15 22:18:20;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/standalone/ld/Makefile,v
Working file: verify/standalone/ld/Makefile
head: 1.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;      selected revisions: 1
description:
Aunit tests, for use with perfect memory for operands.
-----
revision 1.24
date: 1995/05/15 22:17:24;  author: lisar;  state: Exp;  lines: +15 -72
Tidied the Makefile. No functional change.
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/cerbrupttest.S,v
Working file: verify/standalone/uu/cerbrupttest.S
head: 8.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 8.5
date: 1995/05/18 23:42:54;  author: jeffm;  state: Exp;  lines: +4 -3
cerbrupttest - using wrong bit for forced rupt.
exalignharder - use fail instead of mfail
exgenhandler - use fail instead of mfail (was causing hang)
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/exalignharder.S,v
Working file: verify/standalone/uu/exalignharder.S
head: 6.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 6.5
date: 1995/05/18 23:42:56;  author: jeffm;  state: Exp;  lines: +3 -3
cerbrupttest - using wrong bit for forced rupt.
exalignharder - use fail instead of mfail
exgenhandler - use fail instead of mfail (was causing hang)
=====

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/exgenhandler.S,v
Working file: verify/standalone/uu/exgenhandler.S
head: 6.5
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 5;      selected revisions: 1
description:
-----
revision 6.5
date: 1995/05/18 23:42:57;  author: jeffm;  state: Exp;  lines: +8 -8
cerbrupttest - using wrong bit for forced rupt.
exalignharder - use fail instead of mfail
exgenhandler - use fail instead of mfail (was causing hang)
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/.cvsignore,v
Working file: verify/toplevel/.cvsignore
head: 26.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 26.3
date: 1995/05/19 00:34:12;  author: jeffm;  state: Exp;  lines: +2 -0
Added all them aweful .hermes* files to the .cvsignore.
Removed the nasty tests from the Makefile.
Checked in the smaller prblm_debug.sig.
Fixed several tests.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v
Working file: verify/toplevel/BOM
head: 44.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;      selected revisions: 4
description:
releasebom adding BOM
-----
revision 37.0
date: 1995/05/18 19:09:44;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel

Release removal of the nasties
-----
revision 36.1
date: 1995/05/18 19:09:35;  author: lisar;  state: Exp;  lines: +3 -11
releasebom: File needs to be up-to-date to use commit -r
-----
revision 36.0
date: 1995/05/15 20:43:28;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel
```

Fixed cerberus gtlb entry for work for \_2 versions of memory management tests.  
Added cachenasty5 and hermnasty.  
Fixed Makefile for config1 rules.

-----  
revision 35.1  
date: 1995/05/15 20:43:20; author: lisar; state: Exp; lines: +63 -25  
releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v  
Working file: verify/toplevel/Makefile  
head: 1.185  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 185; selected revisions: 2  
description:  
-----  
revision 1.160  
date: 1995/05/19 00:34:16; author: jeffm; state: Exp; lines: +4 -4  
Added all them aweful .hermes\* files to the .cvsignore.  
Removed the nasty tests from the Makefile.  
Checked in the smaller prblm debug.sig.  
Fixed several tests.  
-----

revision 1.159  
date: 1995/05/15 20:35:57; author: lisar; state: Exp; lines: +77 -81  
Tidied up Makefile. Fixed config1 rules.  
Bug fix in hermes\_Ibash.S - still broken though.  
Accessing event register when shouldn't be?  
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcachearnoying.S,v  
Working file: verify/toplevel/dcachearnoying.S  
head: 23.8  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 8; selected revisions: 1  
description:  
-----  
revision 23.8  
date: 1995/05/15 16:22:09; author: jeffm; state: Exp; lines: +4 -16  
Code to turn on dram was not being executed.  
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/doublemctest.S,v  
Working file: verify/toplevel/doublemctest.S  
head: 26.8  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 8; selected revisions: 1  
description:  
-----  
revision 26.5  
date: 1995/05/19 00:34:20; author: jeffm; state: Exp; lines: +4 -8  
=====

Added all them aweful .hermes\* files to the .cvsignore.  
Removed the nasty tests from the Makefile.  
Checked in the smaller prblm\_debug.sig.  
Fixed several tests.

---

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dramprint.S,v  
Working file: verify/toplevel/dramprint.S  
head: 11.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3; selected revisions: 1  
description:  
-----  
revision 11.3  
date: 1995/05/19 00:34:22; author: jeffm; state: Exp; lines: +2 -7  
Added all them aweful .hermes\* files to the .cvsignore.  
Removed the nasty tests from the Makefile.  
Checked in the smaller prblm\_debug.sig.  
Fixed several tests.

---

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dramprintharder.S,v  
Working file: verify/toplevel/dramprintharder.S  
head: 31.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3; selected revisions: 1  
description:  
-----  
revision 31.3  
date: 1995/05/19 00:34:24; author: jeffm; state: Exp; lines: +2 -6  
Added all them aweful .hermes\* files to the .cvsignore.  
Removed the nasty tests from the Makefile.  
Checked in the smaller prblm\_debug.sig.  
Fixed several tests.

---

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes\_Ibash.S,v  
Working file: verify/toplevel/hermes\_Ibash.S  
head: 35.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 2  
description:  
-----  
revision 35.3  
date: 1995/05/18 19:06:37; author: lisar; state: Exp; lines: +9 -9  
Use different registers  
-----  
revision 35.2

```
date: 1995/05/15 20:35:59; author: lisar; state: Exp; lines: +26 -33
Tidied up Makefile. Fixed config1 rules.
Bug fix in hermes_Ibash.S - still broken though.
Accessing event register when shouldn't be?
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/Attic/hermnasty.S,v
Working file: verify/toplevel/hermnasty.S
head: 35.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:
-----
revision 35.3
date: 1995/05/15 18:55:20; author: jeffm; state: Exp; lines: +2 -2
Multiple gltb hits caused test to go X.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/nbsmalltest.S,v
Working file: verify/toplevel/nbsmalltest.S
head: 37.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:
-----
revision 37.1
date: 1995/05/19 00:34:29; author: jeffm; state: Exp;
Added all them aweful .hermes* files to the .cvsignore.
Removed the nasty tests from the Makefile.
Checked in the smaller prblm_debug.sig.
Fixed several tests.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/prblm_debug.sig,v
Working file: verify/toplevel/prblm_debug.sig
head: 33.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7; selected revisions: 1
description:
-----
revision 33.7
date: 1995/05/19 00:34:32; author: jeffm; state: Exp; lines: +1 -27
Added all them aweful .hermes* files to the .cvsignore.
Removed the nasty tests from the Makefile.
Checked in the smaller prblm_debug.sig.
Fixed several tests.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/snoop.S,v
Working file: verify/toplevel/snoop.S
head: 7.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 7.5
date: 1995/05/19 00:34:36;  author: jeffm;  state: Exp;  lines: +24 -26
Added all them aweful .hermes* files to the .cvsignore.
Removed the nasty tests from the Makefile.
Checked in the smaller prblm_debug.sig.
Fixed several tests.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;      selected revisions: 3
description:
-----
revision 1.89
date: 1995/05/18 19:06:31;  author: lisar;  state: Exp;  lines: +74 -80
Use different registers
-----
revision 1.88
date: 1995/05/15 20:44:11;  author: jeffm;  state: Exp;  lines: +9 -9
Moved nasty test to the nasty dir.
-----
revision 1.87
date: 1995/05/15 20:36:04;  author: lisar;  state: Exp;  lines: +33 -32
Tidied up Makefile. Fixed config1 rules.
Bug fix in hermes_Ibash.S - still broken though.
Accessing event register when shouldn't be?
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/xresist.S,v
Working file: verify/toplevel/xresist.S
head: 30.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;      selected revisions: 1
description:
-----
revision 30.4
date: 1995/05/19 00:34:38;  author: jeffm;  state: Exp;  lines: +23 -3
Added all them aweful .hermes* files to the .cvsignore.
Removed the nasty tests from the Makefile.
=====
```

Checked in the smaller prblm\_debug.sig.  
Fixed several tests.

---

```
RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390; selected revisions: 19
description:
top level verilog BOM
-----
revision 3.590
date: 1995/05/18 18:58:15; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
    Makefile.vo
```

This missed BOM 307 but is needed for a good top level run

---

```
revision 3.589
date: 1995/05/18 08:04:39; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
```

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.

cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
Also add pad tick to write enable skew margin.

Power up CTI RAM read index from f4s to f24s per recent analysis.

```
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.
```

ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors  
in the hz to cdio strNdx path; while at it making ctiod receiver of same hr  
too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.

euterpe.V: Remove stale >>>'s per tbr request.

euterpe.status: Add silly logic note on CTIOD tau/eta usage.

Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.

Add note on GTLB NB priority for cache maintenance.

Add note on BGate(I) updates of privilege level relative to GTLB permissions.

Add notes on I & D write/read conflicts and resolution thereof.

Fix notes on illegal sub-octlet stores.

---

```
revision 3.588
date: 1995/05/18 07:20:21; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg
```

avoid toplevel collisions at 900ps

---

```
revision 3.587
```

```
date: 1995/05/18 07:18:28; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions at 900ps
-----
revision 3.586
date: 1995/05/18 07:16:27; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions at 900ps
-----
revision 3.585
date: 1995/05/18 07:14:44; author: dickson; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions at 900ps
-----
revision 3.584
date: 1995/05/17 22:26:47; author: woody; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

Placement change to help top-level routing. Reduced congestion in center area
around instUR/nb dependency stuff. Used up more of the empty space in the first
4 rows.

Atoms:          count atom  bjt  isrc  pld  clock
BJT Totals:    3834  27758  59276  45685  38424  18136

**** converged in 3 iterations ****
-----
revision 3.583
date: 1995/05/17 00:53:15; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctioi

ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up RAM read index from f4s to f24s per recent analysis.
-----
revision 3.582
date: 1995/05/16 22:43:18; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cj

Last release was supposed to be dot-zero.
-----
revision 3.581
date: 1995/05/16 22:40:09; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
  cust_intf.wkz

cj/cj.pim cj/genptab.pl cust_intf.wkz
-----
revision 3.580
date: 1995/05/16 22:39:13; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cj
  cj.pim
  genptab.pl

cj/cj.pim cj/genptab.pl cust_intf.wkz:
```

```
Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
-----
revision 3.579
date: 1995/05/16 08:02:48; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

Part of cdio/ctiod/euterpe.V checkin.
~

-----
revision 3.578
date: 1995/05/16 07:58:34; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cdio

Part of cdio/ctiod/euterpe.V checkin.
~

-----
revision 3.577
date: 1995/05/16 05:01:23; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
    Makefile.vo

deleted obsolete .hwc rule. remove rsh from all gards jobs
-----
revision 3.576
date: 1995/05/16 01:55:13; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
    uu_control.pim

uu/uu_control.pim: Placement for recent uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn.
-----
revision 3.575
date: 1995/05/16 01:07:13; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
    uu.V
    uuprblmr13.Veqn
    uuprblmwm.Veqn

uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:
    Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode
    was forgotten, allowing the PC to increment before being saved by event entry.
    Test cachenasty5_0 noticed with a D cache miss hiccup. Placement later.
-----
revision 3.574
date: 1995/05/13 17:58:39; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Consolidate to .0 BOM for next major snapshot update.

Several small placement tweaks (this version might make it through
second iteration placement . . .).

Tau phase bug fix in uu - this is a logic change.
-----
revision 3.573
date: 1995/05/13 17:40:24; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf
```

```

shift left 18 atoms to prevent clash with cr
-----
revision 3.572
date: 1995/05/13 12:33:07; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
    Makefile.tst

correct syntax error in last change
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737; selected revisions: 21
description:
-----
revision 307.1
date: 1995/05/18 18:57:56; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
    Makefile.vo

This missed BOM 307 but is needed for a good top level run
-----
revision 307.0
date: 1995/05/18 08:04:22; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through
register writes of src!=dst GGFMul to allow NB load data return preempt
to satisfy dependency of only the 2nd high half of a GGFMul source register
pair. Create a hole in GGFMul's repel state to do this. The april95 version
of the nbusemul_0 test noticed in case7. Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
    Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
    Also add pad tick to write enable skew margin.
    Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
    eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and
    .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
    in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
    too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.
euterpe.V: Remove stale >>>'s per tbr request.
euterpe.status: Add silly logic note on CTIOD tau/eta usage.
    Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
    Add note on GTLB NB priority for cache maintenance.
    Add note on BGate(I) updates of privilege level relative to GTLB permissions.
    Add notes on I & D write/read conflicts and resolution thereof.
    Fix notes on illegal sub-octlet stores.
-----
revision 306.15

```

date: 1995/05/18 08:04:11; author: mws; state: Exp; lines: +18 -18  
releasebom: File needs to be up-to-date to use commit -r

-----  
revision 306.14

date: 1995/05/18 07:20:02; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions at 900ps

-----  
revision 306.13

date: 1995/05/18 07:18:08; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions at 900ps

-----  
revision 306.12

date: 1995/05/18 07:16:02; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions at 900ps

-----  
revision 306.11

date: 1995/05/18 07:14:23; author: dickson; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions at 900ps

-----  
revision 306.10

date: 1995/05/17 22:26:32; author: woody; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/uu

Placement change to help top-level routing. Reduced congestion in center area  
around instUR/nb dependency stuff. Used up more of the empty space in the first  
4 rows.

Atoms:	count	atom	bjt	isrc	pld	clock
BJT Totals:	3834	27758	59276	45685	38424	18136

\*\*\*\*\* converged in 3 iterations \*\*\*\*\*

-----  
revision 306.9

date: 1995/05/17 00:52:56; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/ctioi

ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:

Power up RAM read index from f4s to f24s per recent analysis.

-----  
revision 306.8

date: 1995/05/16 22:43:02; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cj

Last release was supposed to be dot-zero.

-----  
revision 306.7

date: 1995/05/16 22:39:48; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc  
cust\_intf.wkz

```
cj/cj.pim cj/genptab.pl cust_intf.wkz
-----
revision 306.6
date: 1995/05/16 22:38:58; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cj
    cj.pim
    genptab.pl

cj/cj.pim cj/genptab.pl cust_intf.wkz:
    Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
-----
revision 306.5
date: 1995/05/16 08:02:29; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

Part of cdio/ctiod/euterpe.V checkin.
~

-----
revision 306.4
date: 1995/05/16 07:58:19; author: billz; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/cdio

Part of cdio/ctiod/euterpe.V checkin.
~

-----
revision 306.3
date: 1995/05/16 05:01:05; author: tbr; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
    Makefile.vo

deleted obsolete .hwc rule. remove rsh from all gards jobs
-----
revision 306.2
date: 1995/05/16 01:54:46; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
    uu_control.pim

uu/uu_control.pim: Placement for recent uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn.
-----
revision 306.1
date: 1995/05/16 01:06:45; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
    uu.V
    uuprblmr13.Veqn
    uuprblmwm.Veqn

uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:
    Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode
    was forgotten, allowing the PC to increment before being saved by event entry.
    Test cachenasty5_0 noticed with a D cache miss hiccup. Placement later.
-----
revision 306.0
date: 1995/05/13 17:58:14; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

Consolidate to .0 BOM for next major snapshot update.

Several small placement tweaks (this version might make it through second iteration placement . . .).

Tau phase bug fix in uu - this is a logic change.

-----  
revision 305.7

date: 1995/05/13 17:58:02; author: tbr; state: Exp; lines: +3 -2  
releasebom: File needs to be up-to-date to use commit -r

-----  
revision 305.6

date: 1995/05/13 17:40:10; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/gf

shift left 18 atoms to prevent clash with cr

-----  
revision 305.5

date: 1995/05/13 12:32:44; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc  
    Makefile.tst

correct syntax error in last change

-----  
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v

Working file: verilog/bsrc/Makefile

head: 1.255

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 255; selected revisions: 1

description:

-----  
revision 1.243

date: 1995/05/17 06:09:12; author: tbr; state: Exp; lines: +1 -2  
delete obsolete reference to ep1ltop

-----  
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v

Working file: verilog/bsrc/Makefile.tst

head: 40.104

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 104; selected revisions: 1

description:

-----  
revision 40.80

date: 1995/05/13 12:32:13; author: tbr; state: Exp; lines: +8 -8  
correct syntax error in last change

-----  
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.vo,v

Working file: verilog/bsrc/Makefile.vo

```

head: 27.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45;      selected revisions: 2
description:
-----
revision 27.40
date: 1995/05/17 23:02:59;  author: vo;  state: Exp;  lines: +8 -8
added sertriflop and serbiflop to list of cells not to flip .
The build in the snapshot did not have any of these cells flipped by the
auto flipper so we're OK here .
-----
revision 27.39
date: 1995/05/16 05:00:44;  author: tbr;  state: Exp;  lines: +9 -30
deleted obsolete .hwc rule.  remove rsh from all gards jobs
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cust_intf.wkz,v
Working file: verilog/bsrc/cust_intf.wkz
head: 304.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;      selected revisions: 7
description:
-----
revision 304.8
date: 1995/05/19 04:30:17;  author: woody;  state: Exp;  lines: +2 -2
Attempt to fix print range problem.
-----
revision 304.7
date: 1995/05/19 03:20:34;  author: mws;  state: Exp;  lines: +57 -49
cust_intf.wkz: Update D cache/tag style to be like I; add read data wire
delay to read margin formula (a 3 ps nit). Overhaul GTLB, especially
write cycle as old formulas thought all inputs had the same setup time
and were to be treated as 2 tick paths and did not get benefit of multi-
cycle setup controlled by the GI block. Make up some limits on write
enable delay, which DTag violates a little and GTLB massively.
-----
revision 304.6
date: 1995/05/18 21:58:49;  author: billz;  state: Exp;  lines: +6 -6
Shows data cache read access margin is -32 (it's 32 pS over, for
2 cycle read at 926pS) and data tag read access margin is +63.

Topt would compute these numbers as -39, and +55 due to a more
pessimistic RC wire delay.

Note: I am not changing any sizes or layout, just the info
(and formulae) in this spread sheet.
-----
revision 304.5
date: 1995/05/17 03:06:19;  author: mws;  state: Exp;  lines: +2 -2
ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
Power up RAM read index from f4s to f24s per recent analysis.

```

-----  
revision 304.4  
date: 1995/05/16 22:36:33; author: mws; state: Exp; lines: +3 -3  
cj/cj.pim cj/genptab.pl cust\_intf.wkz:  
Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
-----

revision 304.3  
date: 1995/05/16 03:48:16; author: mws; state: Exp; lines: +42 -47  
Minor corrections to I cache & tag gate delays. Gave a write skew  
budget exploiting the 1 tick padding around the write enable to make the  
write skew not look like a violation.  
-----

revision 304.2  
date: 1995/05/15 22:16:01; author: dickson; state: Exp; lines: +8 -8  
filled some of ?'s  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v  
Working file: verilog/bsrc/euterpe.V  
head: 6.431  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 431; selected revisions: 2  
description:  
-----

revision 6.419  
date: 1995/05/18 07:53:41; author: mws; state: Exp; lines: +6 -8  
uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
-----

revision 6.418  
date: 1995/05/16 08:05:53; author: billz; state: Exp; lines: +2 -2  
Part of cdio/ctiod/euterpe.V checkin.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v  
Working file: verilog/bsrc/euterpe.status  
head: 24.83  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 83; selected revisions: 1  
description:  
-----

revision 24.72  
date: 1995/05/18 07:53:44; author: mws; state: Exp; lines: +20 -1  
uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt

to satisfy dependency of only the 2nd high half of a GGFMul source register pair. Create a hole in GGFMul's repel state to do this. The april95 version of the nbusemul\_0 test noticed in case7.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i\_euterpe\_wrap.tb,v  
Working file: verilog/bsrc/i\_euterpe\_wrap.tb  
head: 187.15  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 15; selected revisions: 1  
description:  
-----  
revision 187.9  
date: 1995/05/13 22:10:41; author: lisar; state: Exp; lines: +14 -4  
Snoopy is instantiated but sd not connected. Connecting dummy8 to netsd  
causes sd to go to X.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v  
Working file: verilog/bsrc/at/BOM  
head: 93.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 184; selected revisions: 2  
description:  
releasebom adding BOM  
-----  
revision 89.0  
date: 1995/05/18 07:55:37; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

---

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors  
in the hz to cdio strNdx path; while at it making ctiod receiver of same hr  
too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.

Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 88.1  
date: 1995/05/18 07:55:31; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/genptab.pl,v  
Working file: verilog/bsrc/at/genptab.pl  
head: 3.2  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 2; selected revisions: 1  
description:

---

revision 3.2  
date: 1995/05/18 03:51:55; author: mws; state: Exp; lines: +7 -2  
{at,cdio,cj,ctiod,gt,hz,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check and before new version of TOpt mandates it.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v  
Working file: verilog/bsrc/au/BOM  
head: 44.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 89; selected revisions: 2  
description:

---

revision 42.0  
date: 1995/05/18 07:55:56; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors  
in the hz to cdio strNdx path; while at it making ctiod receiver of same hr

too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 41.1  
date: 1995/05/18 07:55:50; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/power.tab.local,v  
Working file: verilog/bsrc/au/power.tab.local  
head: 14.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 1  
description:  

---

revision 14.4  
date: 1995/05/18 03:56:01; author: mws; state: Exp; lines: +4 -1  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v  
Working file: verilog/bsrc/cc/BOM  
head: 92.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 182; selected revisions: 2  
description:  
releasebom adding BOM  

---

revision 85.0  
date: 1995/05/18 07:56:17; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

---

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,

eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors  
in the hz to cdio strNdx path; while at it making ctiod receiver of same hr  
too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 84.1  
date: 1995/05/18 07:56:10; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/power.tab.local,v  
Working file: verilog/bsrc/cc/power.tab.local  
head: 5.2  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 2; selected revisions: 1  
description:  
-----  
revision 5.2  
date: 1995/05/18 03:56:15; author: mws; state: Exp; lines: +4 -0  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/BOM,v  
Working file: verilog/bsrc/cdio/BOM  
head: 55.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 110; selected revisions: 4  
description:  
releasebom adding BOM  
-----  
revision 54.0  
date: 1995/05/18 07:56:36; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc  
  
uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.

Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors  
in the hz to cdio strNdx path; while at it making ctiod receiver of same hr  
too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 53.1  
date: 1995/05/18 07:56:29; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

---

revision 53.0  
date: 1995/05/16 07:58:04; author: billz; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc/cdio

Part of cdio/ctiod/euterpe.V checkin.

~

---

revision 52.1  
date: 1995/05/16 07:57:58; author: billz; state: Exp; lines: +3 -3  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/cdio.V,v  
Working file: verilog/bsrc/cdio/cdio.V  
head: 1.20  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 20; selected revisions: 1  
description:

---

revision 1.20  
date: 1995/05/16 07:57:27; author: billz; state: Exp; lines: +4 -7  
Part of cdio/ctiod/euterpe.V checkin.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/cdio\_control.pim,v  
Working file: verilog/bsrc/cdio/cdio\_control.pim  
head: 28.5  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 5; selected revisions: 1  
description:

```
-----
revision 28.5
date: 1995/05/16 07:57:29; author: billz; state: Exp; lines: +0 -11
Part of cdio/ctiod/euterpe.V checkin.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/genptab.pl,v
Working file: verilog/bsrc/cdio/genptab.pl
head: 3.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:
-----
revision 3.11
date: 1995/05/18 03:52:19; author: mws; state: Exp; lines: +7 -2
{at,cdio,cj,ctiod,gt,hz,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
    eta) phase so TOpt can check and before new version of TOpt mandates it.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259; selected revisions: 2
description:
-----
revision 119.0
date: 1995/05/16 22:42:43; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/cj

Last release was supposed to be dot-zero.
-----
revision 118.1
date: 1995/05/16 22:38:41; author: mws; state: Exp; lines: +3 -3
Release Target: euterpe/verilog/bsrc/cj
    cj.pim
    genptab.pl

cj/cj.pim cj/genptab.pl cust_intf.wkz:
    Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cj.pim,v
Working file: verilog/bsrc/cj/cj.pim
head: 62.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10; selected revisions: 1
```

```

description:
-----
revision 62.10
date: 1995/05/16 22:36:05; author: mws; state: Exp; lines: +475 -476
cj/cj.pim cj/genptab.pl cust_intf.wkz:
  Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/genptab.pl,v
Working file: verilog/bsrc/cj/genptab.pl
head: 47.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7; selected revisions: 1
description:
-----
revision 47.7
date: 1995/05/16 22:36:08; author: mws; state: Exp; lines: +8 -3
cj/cj.pim cj/genptab.pl cust_intf.wkz:
  Power up RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119; selected revisions: 2
description:
releasebom adding BOM
-----
revision 56.0
date: 1995/05/18 07:57:20; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through
  register writes of src!=dst GGFMul to allow NB load data return preempt
  to satisfy dependency of only the 2nd high half of a GGFMul source register
  pair. Create a hole in GGFMul's repel state to do this. The april95 version
  of the nbusemul_0 test noticed in case7. Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
  Also add pad tick to write enable skew margin.
  Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and
  .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
  in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
  too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.
euterpe.V: Remove stale >>>'s per tbr request.
euterpe.status: Add silly logic note on CTIOD tau/eta usage.

```

Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 55.1  
date: 1995/05/18 07:57:13; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/power.tab.local,v  
Working file: verilog/bsrc/cp/power.tab.local  
head: 5.15  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 15; selected revisions: 1  
description:

---

revision 5.13  
date: 1995/05/18 03:56:28; author: mws; state: Exp; lines: +6 -1  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/BOM,v  
Working file: verilog/bsrc/ctiod/BOM  
head: 31.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 61; selected revisions: 4  
description:  
releasebom adding BOM

---

revision 29.0  
date: 1995/05/18 07:57:38; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors

in the hz to cdio strNdx path; while at it making ctiiod receiver of same hr  
too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIODE tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 28.1  
date: 1995/05/18 07:57:32; author: mws; state: Exp; lines: +3 -3  
releasebom: File needs to be up-to-date to use commit -r

---

revision 28.0  
date: 1995/05/16 08:02:11; author: billz; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc/ctiod

Part of cdio/ctiod/euterpe.V checkin.

~

---

revision 27.1  
date: 1995/05/16 08:02:04; author: billz; state: Exp; lines: +3 -3  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/ctiod.V,v  
Working file: verilog/bsrc/ctiod/ctiod.V

head: 1.11

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 11; selected revisions: 2

description:

---

revision 1.10

date: 1995/05/18 07:36:58; author: mws; state: Exp; lines: +2 -2  
Shell style comment illegal in verilog.

---

revision 1.9

date: 1995/05/16 08:01:42; author: billz; state: Exp; lines: +10 -4  
Part of cdio/ctiod/euterpe.V checkin.

~

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/genptab.pl,v

Working file: verilog/bsrc/ctiod/genptab.pl

head: 1.9

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 9; selected revisions: 1

description:

---

revision 1.7

```
date: 1995/05/18 03:53:31; author: mws; state: Exp; lines: +8 -3
{at,cdio,cj,ctiod,gt,hz,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
    eta) phase so TOpt can check not that new version of TOpt mandates it.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/pimlib.pl,v
Working file: verilog/bsrc/ctiod/pimlib.pl
head: 1.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:
-----
revision 1.11
date: 1995/05/16 08:01:44; author: billz; state: Exp; lines: +5 -2
Part of cdio/ctiod/euterpe.V checkin.
~
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/BOM,v
Working file: verilog/bsrc/ctioi/BOM
head: 28.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56; selected revisions: 2
description:
releasebom adding BOM
-----
revision 28.0
date: 1995/05/17 00:52:38; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/ctioi
ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
    Power up RAM read index from f4s to f24s per recent analysis.
-----
revision 27.1
date: 1995/05/17 00:52:29; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/ctioi.pim,v
Working file: verilog/bsrc/ctioi/ctioi.pim
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10; selected revisions: 1
description:
-----
revision 1.10
date: 1995/05/17 00:51:39; author: mws; state: Exp; lines: +21 -26
```

```
ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up RAM read index from f4s to f24s per recent analysis.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctioi/power.tab.local,v
Working file: verilog/bsrc/ctioi/power.tab.local
head: 4.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 4.7
date: 1995/05/17 00:51:42;  author: mws;  state: Exp;  lines: +12 -8
ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up RAM read index from f4s to f24s per recent analysis.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;      selected revisions: 2
description:
-----
revision 91.0
date: 1995/05/18 07:14:03;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

  avoid toplevel collisions at 900ps
-----
revision 90.1
date: 1995/05/18 07:13:53;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.pim,v
Working file: verilog/bsrc/es/es.pim
head: 5.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;      selected revisions: 1
description:
-----
revision 5.51
date: 1995/05/18 07:12:49;  author: dickson;  state: Exp;  lines: +1 -1
  avoid toplevel collisions at 900ps
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/genpim.pl,v
```

```
Working file: verilog/bsrc/es/genpim.pl
head: 37.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;      selected revisions: 1
description:
-----
revision 37.14
date: 1995/05/18 07:13:02;  author: dickson;  state: Exp;  lines: +3 -3
avoid toplevel collisions at 900ps
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/power.tab.local,v
Working file: verilog/bsrc/es/power.tab.local
head: 13.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 13.7
date: 1995/05/18 03:56:43;  author: mws;  state: Exp;  lines: +4 -1
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/BOM,v
Working file: verilog/bsrc/gf/BOM
head: 37.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 35.0
date: 1995/05/13 17:39:53;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gf

shift left 18 atoms to prevent clash with cr
-----
revision 34.1
date: 1995/05/13 17:39:47;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.pim,v
Working file: verilog/bsrc/gf/gf.pim
head: 4.15
branch:
```

```

locks: strict
access list:
keyword substitution: kv
total revisions: 15;      selected revisions: 1
description:
-----
revision 4.13
date: 1995/05/13 17:39:05;  author: tbr;  state: Exp;  lines: +8 -8
move left 18 atoms to prevent clash with cr
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 93.0
date: 1995/05/18 07:59:10;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through
register writes of src!=dst GGFMul to allow NB load data return preempt
to satisfy dependency of only the 2nd high half of a GGFMul source register
pair. Create a hole in GGFMul's repel state to do this. The april95 version
of the nbusemul_0 test noticed in case7. Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
  Also add pad tick to write enable skew margin.
  Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and
  .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
  in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
  too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.
euterpe.V: Remove stale >>>'s per tbr request.
euterpe.status: Add silly logic note on CTIOD tau/eta usage.
  Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
  Add note on GTLB NB priority for cache maintenance.
  Add note on BGate(I) updates of privilege level relative to GTLB permissions.
  Add notes on I & D write/read conflicts and resolution thereof.
  Fix notes on illegal sub-octlet stores.
-----
revision 92.1
date: 1995/05/18 07:59:03;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/genptab.pl,v
Working file: verilog/bsrc/gt/genptab.pl

```

```
head: 24.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 24.7
date: 1995/05/18 03:53:44;  author: mws;  state: Exp;  lines: +7 -2
{at,cdio,cj,ctiod,gt,hz,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 108.0
date: 1995/05/18 07:15:36;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions at 900ps
-----
revision 107.1
date: 1995/05/18 07:15:26;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/Makefile,v
Working file: verilog/bsrc/hc/Makefile
head: 1.30
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 30;      selected revisions: 1
description:
-----
revision 1.29
date: 1995/05/18 07:14:19;  author: dickson;  state: Exp;  lines: +3 -1
avoid toplevel collisions at 900 ps
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0_control.pim,v
Working file: verilog/bsrc/hc/hc0_control.pim
head: 73.25
branch:
locks: strict
```

```

access list:
keyword substitution: kv
total revisions: 25;      selected revisions: 1
description:
-----
revision 73.15
date: 1995/05/18 07:14:25;  author: dickson;  state: Exp;  lines: +68 -68
avoid toplevel collisions at 900 ps
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/BOM,v
Working file: verilog/bsrc/hz/BOM
head: 30.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 58;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 29.0
date: 1995/05/18 07:59:37;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through
register writes of src!=dst GGFMul to allow NB load data return preempt
to satisfy dependency of only the 2nd high half of a GGFMul source register
pair. Create a hole in GGFMul's repel state to do this. The april95 version
of the nbusemul_0 test noticed in case7. Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
Also add pad tick to write enable skew margin.
Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.
euterpe.V: Remove stale >>>'s per tbr request.
euterpe.status: Add silly logic note on CTIOD tau/eta usage.
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
Add note on GTLB NB priority for cache maintenance.
Add note on BGate(I) updates of privilege level relative to GTLB permissions.
Add notes on I & D write/read conflicts and resolution thereof.
Fix notes on illegal sub-octlet stores.
-----
revision 28.1
date: 1995/05/18 07:59:31;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/power.tab.local,v
Working file: verilog/bsrc/hz/power.tab.local
head: 4.2

```

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 4.2
date: 1995/05/18 03:57:02;  author: mws;  state: Exp;  lines: +8 -0
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 47.0
date: 1995/05/18 07:59:57;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status:  Generalize possibility of interrupt halfway through
  register writes of src!=dst GGFMul to allow NB load data return preempt
  to satisfy dependency of only the 2nd high half of a GGFMul source register
  pair.  Create a hole in GGFMul's repel state to do this.  The april95 version
  of the nbusemul_0 test noticed in case7.  Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
  Also add pad tick to write enable skew margin.
  Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V:  Shell style comment illegal in verilog.  Cdio, ctiod, .V and
  .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
  in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
  too so all paths now 2 ticks.  Euterpe.V was coreq but not in BOMs.
euterpe.V:  Remove stale >>>'s per tbr request.
euterpe.status:  Add silly logic note on CTIOD tau/eta usage.
  Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
  Add note on GTLB NB priority for cache maintenance.
  Add note on BGate(I) updates of privilege level relative to GTLB permissions.
  Add notes on I & D write/read conflicts and resolution thereof.
  Fix notes on illegal sub-octlet stores.
-----
revision 46.1
date: 1995/05/18 07:59:50;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====
```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/power.tab.local,v
Working file: verilog/bsrc/icc/power.tab.local
head: 39.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 39.2
date: 1995/05/18 03:57:13;  author: mws;  state: Exp;  lines: +4 -1
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/BOM,v
Working file: verilog/bsrc/ife/BOM
head: 68.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 140;      selected revisions: 2
description:
-----
revision 68.0
date: 1995/05/18 08:00:19;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status:  Generalize possibility of interrupt halfway through
  register writes of src!=dst GGFMul to allow NB load data return preempt
  to satisfy dependency of only the 2nd high half of a GGFMul source register
  pair.  Create a hole in GGFMul's repel state to do this.  The april95 version
  of the nbusemul_0 test noticed in case7.  Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
  Also add pad tick to write enable skew margin.
  Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V:  Shell style comment illegal in verilog.  Cdio, ctiod, .V and
  .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
  in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
  too so all paths now 2 ticks.  Euterpe.V was coreq but not in BOMs.
euterpe.V:  Remove stale >>>'s per tbr request.
euterpe.status:  Add silly logic note on CTIOD tau/eta usage.
  Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
  Add note on GTLB NB priority for cache maintenance.
  Add note on BGate(I) updates of privilege level relative to GTLB permissions.
  Add notes on I & D write/read conflicts and resolution thereof.
  Fix notes on illegal sub-octlet stores.
-----
revision 67.1

```

```

date: 1995/05/18 08:00:12; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/power.tab.local,v
Working file: verilog/bsrc/ife/power.tab.local
head: 15.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:
-----
revision 15.2
date: 1995/05/18 03:57:24; author: mws; state: Exp; lines: +4 -0
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196; selected revisions: 2
description:
releasebom adding BOM
-----
revision 95.0
date: 1995/05/18 08:00:59; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through
  register writes of src!=dst GGFMul to allow NB load data return preempt
  to satisfy dependency of only the 2nd high half of a GGFMul source register
  pair. Create a hole in GGFMul's repel state to do this. The april95 version
  of the nbusemul_0 test noticed in case7. Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
  Also add pad tick to write enable skew margin.
  Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and
  .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
  in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
  too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.
euterpe.V: Remove stale >>>'s per tbr request.
euterpe.status: Add silly logic note on CTIOD tau/eta usage.
  Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
  Add note on GTLB NB priority for cache maintenance.
  Add note on BGate(I) updates of privilege level relative to GTLB permissions.

```

Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

=====

revision 94.1  
date: 1995/05/18 08:00:50; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/genptab.pl,v  
Working file: verilog/bsrc/lt/genptab.pl  
head: 56.2  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 2; selected revisions: 1  
description:

=====

revision 56.2  
date: 1995/05/18 03:55:04; author: mws; state: Exp; lines: +7 -2  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v  
Working file: verilog/bsrc/mc/BOM  
head: 79.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 157; selected revisions: 2  
description:  
releasebom adding BOM

=====

revision 77.0  
date: 1995/05/18 07:17:47; author: dickson; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc/mc

avoid toplevel collisions at 900ps

=====

revision 76.1  
date: 1995/05/18 07:17:37; author: dickson; state: Exp; lines: +6 -6  
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/Makefile,v  
Working file: verilog/bsrc/mc/Makefile  
head: 1.21  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 21; selected revisions: 1  
description:

=====

```
revision 1.21
date: 1995/05/18 07:16:43; author: dickson; state: Exp; lines: +3 -1
avoid toplevel collisions at 900ps
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/genpim.pl,v
Working file: verilog/bsrc/mc/genpim.pl
head: 13.17
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 17; selected revisions: 1
description:
-----
revision 13.16
date: 1995/05/18 07:16:45; author: dickson; state: Exp; lines: +3 -3
avoid toplevel collisions at 900ps
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataHigh.pim,v
Working file: verilog/bsrc/mc/mc.dataHigh.pim
head: 48.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9; selected revisions: 1
description:
-----
revision 48.9
date: 1995/05/18 07:16:47; author: dickson; state: Exp; lines: +200 -200
avoid toplevel collisions at 900ps
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataLow.pim,v
Working file: verilog/bsrc/mc/mc.dataLow.pim
head: 48.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7; selected revisions: 1
description:
-----
revision 48.7
date: 1995/05/18 07:16:51; author: dickson; state: Exp; lines: +776 -776
avoid toplevel collisions at 900ps
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/power.tab.local,v
Working file: verilog/bsrc/mc/power.tab.local
head: 16.4
branch:
locks: strict
access list:
keyword substitution: kv
```

```

total revisions: 4;      selected revisions: 1
description:
-----
revision 16.4
date: 1995/05/18 03:57:33;  author: mws;  state: Exp;  lines: +4 -1
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
    eta) phase so TOpt can check not that new version of TOpt mandates it.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v
Working file: verilog/bsrc/nb/BOM
head: 130.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 261;  selected revisions: 2
description:
releasebom adding BOM
-----
revision 127.0
date: 1995/05/18 08:01:49;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status:  Generalize possibility of interrupt halfway through
register writes of src!=dst GGFMul to allow NB load data return preempt
to satisfy dependency of only the 2nd high half of a GGFMul source register
pair.  Create a hole in GGFMul's repel state to do this.  The april95 version
of the nbusemul_0 test noticed in case7.  Placement still OK.
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
Also add pad tick to write enable skew margin.
Power up CTI RAM read index from f4s to f24s per recent analysis.
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
    eta) phase so TOpt can check not that new version of TOpt mandates it.
ctiod/ctiod.V:  Shell style comment illegal in verilog.  Cdio, ctiod, .V and
    .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
    in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
    too so all paths now 2 ticks.  Euterpe.V was coreq but not in BOMs.
euterpe.V:  Remove stale >>>'s per tbr request.
euterpe.status:  Add silly logic note on CTIOD tau/eta usage.
    Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.
    Add note on GTLB NB priority for cache maintenance.
    Add note on BGate(I) updates of privilege level relative to GTLB permissions.
    Add notes on I & D write/read conflicts and resolution thereof.
    Fix notes on illegal sub-octlet stores.
-----
revision 126.1
date: 1995/05/18 08:01:42;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/genptab.pl,v
Working file: verilog/bsrc/nb/genptab.pl
head: 52.6

```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 52.6
date: 1995/05/18 03:55:17;  author: mws;  state: Exp;  lines: +7 -2
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;      selected revisions: 2
description:
-----
revision 127.0
date: 1995/05/18 07:19:39;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions at 900ps
-----
revision 126.1
date: 1995/05/18 07:19:28;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/genpim.pl,v
Working file: verilog/bsrc/rg/genpim.pl
head: 19.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;      selected revisions: 1
description:
-----
revision 19.14
date: 1995/05/18 07:18:36;  author: dickson;  state: Exp;  lines: +3 -3
avoid toplevel collisions at 900ps
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/genptab.pl,v
Working file: verilog/bsrc/rg/genptab.pl
head: 82.4
branch:
locks: strict
access list:
keyword substitution: kv
```

```

total revisions: 4;      selected revisions: 1
description:
-----
revision 82.3
date: 1995/05/18 03:55:30;  author: mws;  state: Exp;  lines: +8 -3
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;      selected revisions: 1
description:
-----
revision 82.24
date: 1995/05/18 07:18:40;  author: dickson;  state: Exp;  lines: +36 -36
avoid toplevel collisions at 900ps
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v
Working file: verilog/bsrc/sr/BOM
head: 75.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 71.0
date: 1995/05/18 08:02:39;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status:  Generalize possibility of interrupt halfway through
  register writes of src!=dst GGFMul to allow NB load data return preempt
  to satisfy dependency of only the 2nd high half of a GGFMul source register
  pair.  Create a hole in GGFMul's repel state to do this.  The april95 version
  of the nbusemul_0 test noticed in case7.  Placement still OK.

cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust_intf.wkz:
  Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.
  Also add pad tick to write enable skew margin.
  Power up CTI RAM read index from f4s to f24s per recent analysis.

{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local:  Specify tau (and when present,
  eta) phase so TOpt can check not that new version of TOpt mandates it.

ctiod/ctiod.V:  Shell style comment illegal in verilog.  Cdio, ctiod, .V and
  .pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors
  in the hz to cdio strNdx path; while at it making ctiod receiver of same hr
  too so all paths now 2 ticks.  Euterpe.V was coreq but not in BOMs.

euterpe.V:  Remove stale >>>'s per tbr request.

```

euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

---

revision 70.1  
date: 1995/05/18 08:02:33; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/genptab.pl,v  
Working file: verilog/bsrc/sr/genptab.pl  
head: 27.7  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 7; selected revisions: 1  
description:

---

revision 27.7  
date: 1995/05/18 03:55:42; author: mws; state: Exp; lines: +7 -2  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v  
Working file: verilog/bsrc/uu/BOM  
head: 218.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 480; selected revisions: 6  
description:

---

revision 200.0  
date: 1995/05/18 08:03:19; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through  
register writes of src!=dst GGFMul to allow NB load data return preempt  
to satisfy dependency of only the 2nd high half of a GGFMul source register  
pair. Create a hole in GGFMul's repel state to do this. The april95 version  
of the nbusemul\_0 test noticed in case7. Placement still OK.  
cj/cj.pim cj/genptab.pl ctioi/ctioi.pim ctioi/power.tab.local cust\_intf.wkz:  
Power up CI RAM read index 5:0 (ifp 9:4) from f8s to f12s per recent analysis.  
Also add pad tick to write enable skew margin.  
Power up CTI RAM read index from f4s to f24s per recent analysis.  
{at,cdio,cj,ctiod,gt,lt,nb,rg,sr}/genptab.pl: \  
{au,cc,cp,es,hz,icc,ife,mc,uu}/power.tab.local: Specify tau (and when present,  
eta) phase so TOpt can check not that new version of TOpt mandates it.  
ctiod/ctiod.V: Shell style comment illegal in verilog. Cdio, ctiod, .V and  
.pim changes in bsrc BOM's 306.5 and 306.4 were fixing hr/tau phase errors

in the hz to cdio strNdx path; while at it making ctiod receiver of same hr too so all paths now 2 ticks. Euterpe.V was coreq but not in BOMs.  
euterpe.V: Remove stale >>>'s per tbr request.  
euterpe.status: Add silly logic note on CTIOD tau/eta usage.  
Add note on "a" wires leaving HZ for heavy loads but also srcing local logic.  
Add note on GTLB NB priority for cache maintenance.  
Add note on BGate(I) updates of privilege level relative to GTLB permissions.  
Add notes on I & D write/read conflicts and resolution thereof.  
Fix notes on illegal sub-octlet stores.

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revision 199.1  
date: 1995/05/18 08:03:12; author: mws; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

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revision 199.0  
date: 1995/05/17 22:26:16; author: woody; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc/uu

Placement change to help top-level routing. Reduced congestion in center area around instUR/nb dependency stuff. Used up more of the empty space in the first 4 rows.

Atoms: count atom bjt isrc pld clock  
BJT Totals: 3834 27758 59276 45685 38424 18136

\*\*\*\* converged in 3 iterations \*\*\*\*

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revision 198.3  
date: 1995/05/17 22:26:08; author: woody; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

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revision 198.2  
date: 1995/05/16 01:54:19; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/uu  
uu\_control.pim

uu/uu\_control.pim: Placement for recent uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn.

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revision 198.1  
date: 1995/05/16 01:06:13; author: mws; state: Exp; lines: +4 -4  
Release Target: euterpe/verilog/bsrc/uu  
uu.V  
uuprblmr13.Veqn  
uuprblmwm.Veqn

uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:

Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode was forgotten, allowing the PC to increment before being saved by event entry. Test cachenasty5\_0 noticed with a D cache miss hiccup. Placement later.

---

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v  
Working file: verilog/bsrc/uu/uu.V  
head: 1.202  
branch:  
locks: strict  
access list:

```

keyword substitution: kv
total revisions: 202; selected revisions: 2
description:
issue unit
-----
revision 1.190
date: 1995/05/18 07:54:25; author: mws; state: Exp; lines: +11 -2
uu/uu.V euterpe.status: Generalize possibility of interrupt halfway through
register writes of src!=dst GGFMul to allow NB load data return preempt
to satisfy dependency of only the 2nd high half of a GGFMul source register
pair. Create a hole in GGFMul's repel state to do this. The april95 version
of the nbusemul_0 test noticed in case7. Placement still OK.
-----
revision 1.189
date: 1995/05/16 01:05:07; author: mws; state: Exp; lines: +4 -4
uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:
Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode
was forgotten, allowing the PC to increment before being saved by event entry.
Test cachenasty5_0 noticed with a D cache miss hiccup. Placement later.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60; selected revisions: 2
description:
-----
revision 68.53
date: 1995/05/17 22:22:53; author: woody; state: Exp; lines: +3161 -3093
Placement change to help top-level routing. Reduced congestion in center area
around instUR/nb dependency stuff. Used up more of the empty space in the first
4 rows.

Atoms:           count atom   bjt   isrc   pld   clock
      BJT Totals: 3834 27758 59276 45685 38424 18136

**** converged in 3 iterations ****
-----
revision 68.52
date: 1995/05/16 01:53:03; author: mws; state: Exp; lines: +9 -12
uu/uu_control.pim:
Placement for recent uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn.
Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode
was forgotten, allowing the PC to increment before being saved by event entry.
Test cachenasty5_0 noticed with a D cache miss hiccup.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr13.Veqn,v
Working file: verilog/bsrc/uu/uuprblmr13.Veqn
head: 60.11
branch:
locks: strict
access list:

```

```
keyword substitution: kv
total revisions: 11;      selected revisions: 1
description:
-----
revision 60.11
date: 1995/05/16 01:05:18;  author: mws;  state: Exp;  lines: +27 -2
uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:
  Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode
  was forgotten, allowing the PC to increment before being saved by event entry.
  Test cachenasty5_0 noticed with a D cache miss hiccup.  Placement later.
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmwm.Veqn,v
Working file: verilog/bsrc/uu/uuprblmwm.Veqn
head: 50.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;      selected revisions: 1
description:
-----
revision 50.18
date: 1995/05/16 01:05:22;  author: mws;  state: Exp;  lines: +32 -22
uu/uuprblmr13.Veqn uu/uuprblmwm.Veqn uu/uu.V:
  Once a rupt was decided to be taken on eta2 jobs, any hiccup/xcptn it overrode
  was forgotten, allowing the PC to increment before being saved by event entry.
  Test cachenasty5_0 noticed with a D cache miss hiccup.  Placement later.
=====
```